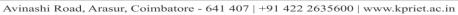


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M.E VLSI DESIGN **REGULATIONS – 2019** CHOICE BASED CREDIT SYSTEM

CURRICULUM FOR I TO II SEMESTERS

SEMESTER I

SL.NO.	COURSE CODE	COURSE TITLE	CATEGORY	L	T	P	C	
THEORY	THEORY							
1	P19VL101	Analog Integrated Circuits Design	PC	3	0	0	3	
2	P19VL102	Digital CMOS VLSI Design	PC	3	0	0	3	
3		Professional Elective I	PE	3	0	0	3	
4		Professional Elective II	PE	3	0	0	3	
5	P19VL103	Research Methodology	HSM	3	0	0	3	
PRACTIO	PRACTICALS							
6	P19VL104	VLSI Design Laboratory I	PC	0	0	4	2	
7	P19VL105	VLSI Design Laboratory II	PC	0	0	4	2	
			TOTAL	15	0	8	19	

SEMESTER II

SL.NO	COURSE CODE	COURSE TITLE	CATEGORY	L	T	P	C	
THEORY	7							
1	P19VL201	Low Power VLSI Design	PC	3	0	0	3	
2	P19VL202	Testing for VLSI Circuits	PC	3	0	0	3	
3		Professional Elective III	PE	3	0	0	3	
4		Professional Elective IV	PE	3	0	0	3	
PRACTIO	PRACTICALS							
5	P19VL203	VLSI Design Laboratory III	PC	0	0	4	2	
6	P19VL204	VLSI Design Laboratory IV	PC	0	0	4	2	
7	P19VL205	Mini Project with Seminar	EEC	0	0	4	2	
	•		TOTAL	12	0	12	18	



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PROFESSIONAL ELECTIVES (PE)

SEMESTER I

ELECTIVE I

SL.NO.	COURSE CODE	COURSE TITLE	L	T	P	C
1	P19VLP01	CAD for VLSI Circuits	3	0	0	3
2	P19VLP02	VLSI Physical Design	3	0	0	3
3	P19VLP03	Scripting Language for VLSI	3	0	0	3

SEMESTER I

ELECTIVE II

SL.NO.	COURSE CODE	COURSE TITLE	L	T	P	C
1	P19VLP04	Advanced Digital System Design	3	0	0	3
2	P19VLP05	ASIC and FPGA Design	3	0	0	3
3	P19VLP06	System Verilog	3	0	0	3

SEMESTER II

ELECTIVE III

SL.NO.	COURSE CODE	COURSE TITLE	L	T	P	C
1	P19VLP07	Optimization Algorithm for VLSI	3	0	0	3
2	P19VLP08	Semiconductor Device Modeling	3	0	0	3
3	P19VLP09	Interconnections and Packaging for VLSI	3	0	0	3

SEMESTER II

ELECTIVE IV

SL.NO.	COURSE CODE	COURSE TITLE	L	T	P	C
1	P19VLP10	Hardware Verification Techniques	3	0	0	3
2	P19VLP11	IP based VLSI	3	0	0	3
3	P19VLP12	MEMS & NEMS	3	0	0	3